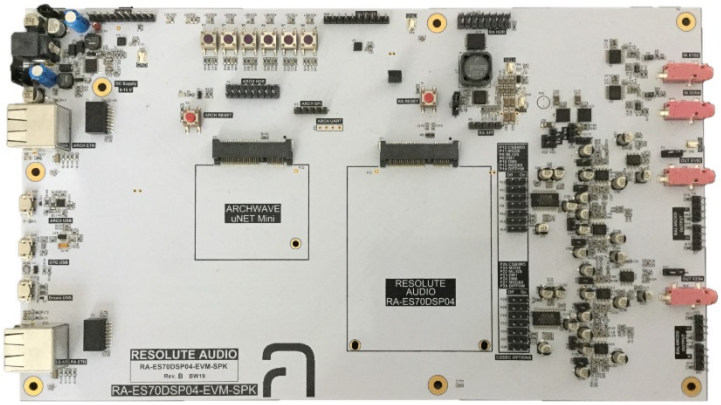
RA-ES70DSP04-EVM

DEVELOPMENT BOARD FOR AES70 CONTROLLED DSP AND AES67 AUDIO OVER IP

Applications

- *Networked Speakers*
- *Pro-audio Amplifiers*
- *Distribution Amplifiers*
- *Conference Systems*
- *Networked Microphones*
- *Networked Effects Gear*



Revision History

Version	Date	Description
0.01	01/05/2020	Draft datasheet

Disclaimer

Table of Contents

RA-ES70DSP04-EVM

General Description

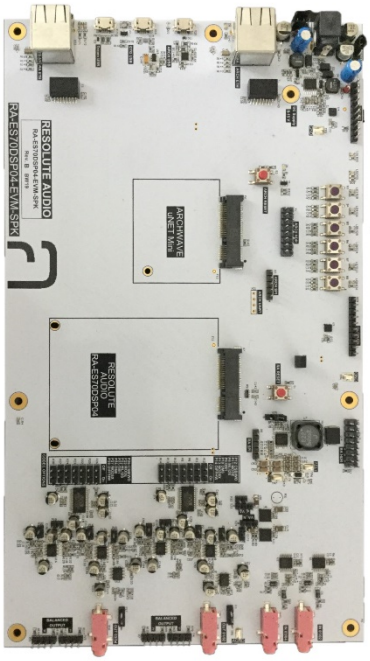
The RA-ES70DSP04-EVM is a development board that enables rapid prototyping of products that require AES70 control and/or AES67 audio over IP. It includes everything needed to get up and running quickly and easily, including an RA-ES70DSP04 DSP module for AES70 control of the DSP functions, and an uNET mini module from Archwave for streaming AES67 audio. There are two AES67 AoIP channels in and out, plus four analog inputs and outputs. The analog outputs are presented as single ended on 3mm head-phone jacks as well as high quality balanced outputs on separate headers.

All the voltage rails are generated on board from a single input, including very low ripple supplies for the analog stages. There are six switches and eight LEDs providing GPIO functions, as well as three USB interfaces. Ample headers are on-board to access all the key signals for testing and connecting to external circuitry.

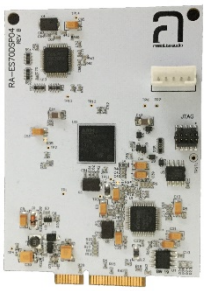
The board is pre-loaded with test firmware for a quick start demonstration and evaluation.

EVM KIT Contents

- *RA-ES70DSP04-EVM Board*
- *RA-ES70DSP04 module*
- *uNET-mini module*
- *Power supply 12VDC Output, 1A, 5.5x2.1x12mm*
- *EU version TRE15120-E-11G03-Level-VI*
- *UK version TRE15120-U-11G03-Level-VI*
- *STM programmer ST-LINK/V2*
- *JTAG adapter Olimex ARM-JTAG-20-10*
- *DREAM programmer SAM5000-DBG-IF*
- *2x CAT6 cable*



RA-ES70DSP04-EVM

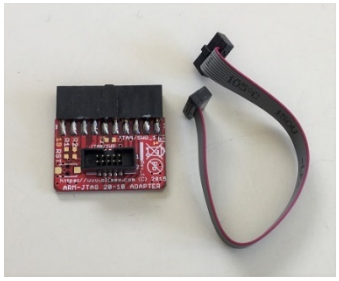


RA-ES70DSP04

uNET-mini module

ST-LINK/V2

SAM5000-DBG-IF

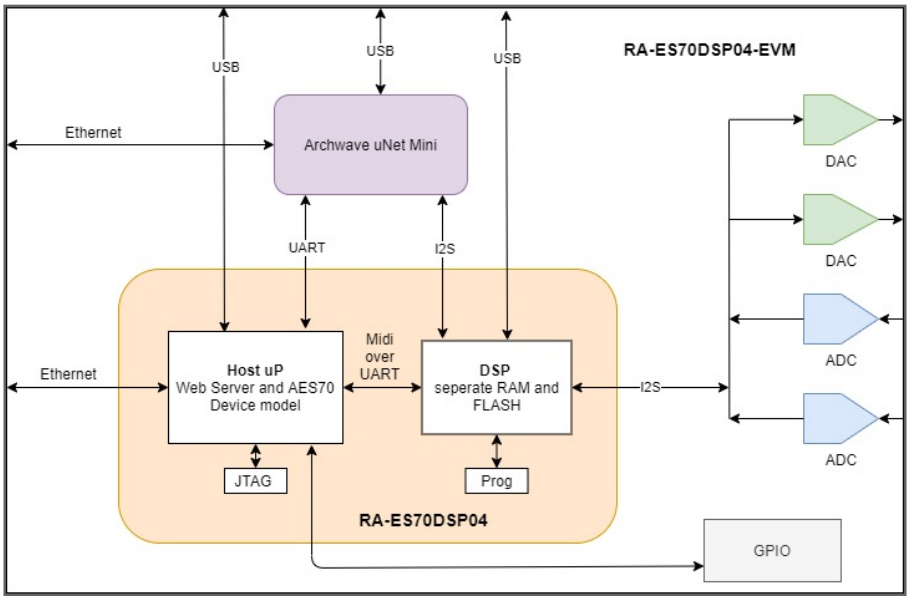


Olimex ARM-JTAG-20-10

Power supply 12VDC

CAT6 cable

Block Diagram



Operation

The RA-ES70DSP04-EVM development board has been designed to accommodate the RA-ES70DSP04 AES70 module and the Archwave AES67 module to ease the AES70 product development process and demonstrate a complete system featuring an AES67 digital audio source, an AES70 control system and webserver interface.

On receiving this board development kit, the RA-ES70DSP04 module is discoverable using the static IP address 192.168.1.10.

Test Firmware User Guide

Both example firmware files allow audio to be input to the RA-ES70DSP04-EVM via 3.5mm stereo jack sockets X10 and X11 and output can be heard at X15 and X16.

X10L → X15L

X10L → X15R

X11L → X16L

X11R → X16R

The buttons and LEDS on the RA-ES70DSP04-EVM correspond to the GPIO window in the webserver interface. Selecting the LED buttons will activate the LED on the board while pressing a button on the board will activate the icon in the web browser.

The effects block allow the user to make value changes to the DSP settings to the corresponding audio channel.

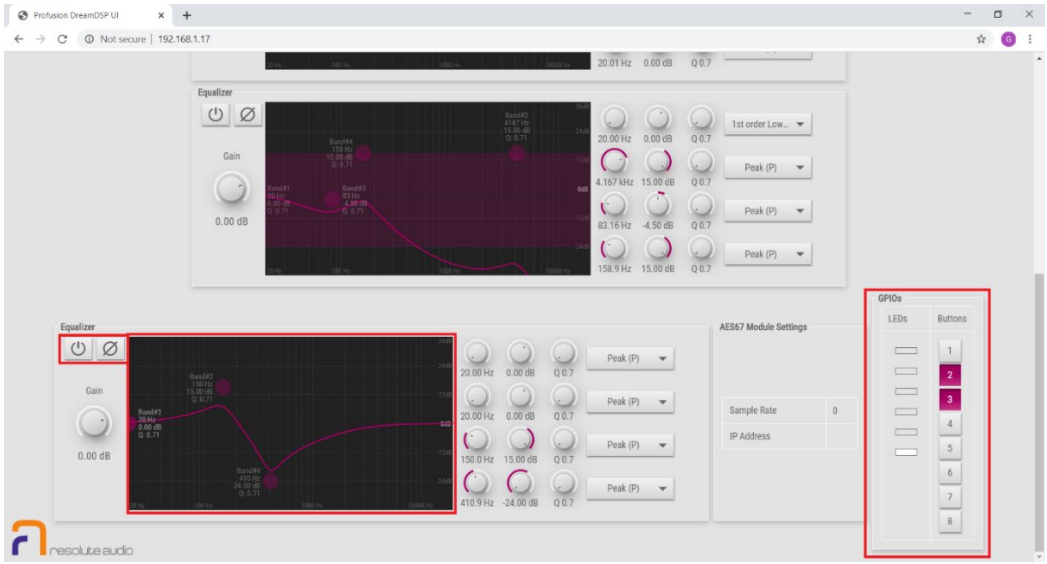


Figure 1 - AES70 Webserver Control Interface for the Biquad Example Application

Electrical Characteristics

Measured at ambient temperature 25ºC

PARAMETER	*CONDITIONS*	*Min.*	*Typ.*	*Max.*	*Units*
Input Voltage					V
Input Current	Typical use		290		mA
Input Current start-up	High load		470		mA
Input Current VAP/VAN removed			26		mA
Input Current P34 removed			19		mA
Time from Power to MCU Reset			4		ms
PSU Ripple +3.3V @175 MHz BW			46		mV
IO Expander Latency			TBC		ms
Output stage Levels			TBC		mV
Output Stage THD+N			TBC		%
Input stage Levels			TBC		mV
Input Stage THD+N			TBC		%
Total Loopback delay			0.96		ms
Loopback Latency ADC-DAC			0.87		ms

CONNECTIVITY AND PIN DESCRIPTIONS

X7 RA-ES70DSP04 Edge Connector

Pin	Net	Pin Description
1,2,3,4	5VD	+5V supply
5,6,7,8	GND	0V ground
9	MCU_SPI_NCS0	SPI interface. The SPI can run in slave and master modes in full-duplex and simplex communication modes. It can communicate at up to 15 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.
10	RXD0	Receive pin of universal synchronous/asynchronous receiver transmitter(USART). Supports up to 7.5Mbit/s.
11	MCU_SPI_SCK	SPI Interface see pin 9
12	TXD0	Transmit pin of universal synchronous/asynchronous receiver transmitter(USART). Supports up to 7.5Mbit/s.
13	MCU_SPI_MOSI	SPI Interface see pin 9
14	RESET_MOD	Configurable GPIO
15	MCU_SPI_MISO	SPI Interface see pin 9
16	AUDIO_OUT_3	I2S output
17	GPIO(DAC_MUTE)	Configurable GPIO pin PH14 on MCU. (Used for DAC_MUTE on the RA-ES70DSP04-EVM board)
18	RA_ETH_RD_P	Ethernet PHY differential receive input (PMD Input Pair). These differential inputs are automatically configured to accept either 100BASE-TX or 10BASE-Tsignaling.
19	RESET_RA	Reset pin. When pulled low it will reset host processor, DSP, PHY and the JTAG.

20	RA_ETH_RD_N	Ethernet PHY signal requiring external magnetics. See pin 18
21	GPIO(NRESET_CODEC)	Configurable GPIO pin PH12 on MCU. (Used for NRESET_CODEC on the RA-ES70DSP04-EVM board)
22	RA_ETH_TD_P	Ethernet PHY differential common driver transmit output (PMD Output Pair). These different outputs are automatically configured to either 10BASE-T or 100BASE-TX signalling.
23	I2C_SCL	I2C Clock pin. The interface can operate in multimaster and slave modes, and can support the Standard- and Fast-modes. Supports the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.
24	RA_ETH_TD_N	Ethernet PHY signal requiring external magnetics. See pin 22
25	I2C_SDA	I2C Data pin. See pin 23
26	GND	0V ground
27	DREAM_MCLK	DSP master clock output.
28	RA_ETH_LED_A	LINK LED: This pin indicates the status of the LINK. The LED will be ON when Link is good.
29	AUDIO_OUT_1	I2S output
30	RA_ETH_LED_B	ACTIVITY LED: This pin is the Activity LED which is ON when activity is present on either Transmit or Receive.
31	AUDIO_IN_1	I2S input
32	IO_INT	Configurable GPIO from pin PI2 on MCU. Nominally programmed as GPIO expander interrupt
33	AUDIO_OUT_2	I2S output
34	OTG_FS_ID	Universal serial bus on-the-go full-speed (OTG_FS) from MCU. USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume.
35,36	GND	0V ground
37	SDATAIN	I2S Input

38	DREAM_USB_P	USB 2.0 High-Speed port from DSP. It can be used as Device, Host or Dual Role
39	GPIO	Configurable GPIO pin
40	DREAM_USB_N	USB 2.0 High-Speed port from DSP. It can be used as Device, Host or Dual Role
41	SDATAOUT	I2S Output
42	OTG_FS_USB_P	USB on-the-go full-speed (OTG_FS) from MCU. See pin 34
43	AUDIO_IN_2	I2S input
44	OTG_FS_USB_N	USB on-the-go full-speed (OTG_FS) from MCU. See pin 34
45,46	GND	0V ground
47	MCLK	Incoming Master Clock to synchronise the DSP to I2S audio streams
48	OTG_FS_OverCurrent	USB on-the-go full-speed (OTG_FS) from MCU.
49	DREAM_SCLK	DSP bit clock output for I2S Note: FS1 Pin sensed at power up. FS1|FS0 allows boot ROM code to know operating freq. on oscillator OSC1 as follows: 00->12MHz(Default) 01->9.6MHz, 10->11.2896MHz, 11->12.288MHz
50	OTG_FS_PowerSwitchOn	Universal serial bus on-the-go full-speed (OTG_FS) from MCU. See pin 34
51	LRCK	DSP word clock. Output by default. Input if external device used. Note: FS0 Sensed at power up. FS1|FS0 allows boot ROM code to know operating freq on OSC1 (see FS1)
52	VBUS_FS	VBUS for USB Full-Speed(FS) On-The-Go(OTG) port

HEADERS

X3 – RA Header

Pin	Signal	Direction	Description
1	DAC_MUTE	I	0 = Mute DAC outputs 1 = Normal operation
2	AUDIO_IN_1	I	I2S input
3	IO_INT	O	Interrupt pin from STMPE811 of U4
4	AUDIO_OUT_1	O	I2S output
5	NRESET_CODEC	I	0 = MUTE ADC and DAC 1 = Normal operation
6	3V3	POWER	
7	I2C_SCL	O	I2C Clock pin.
8	LRCK	I/O	DSP word clock.
9	I2C_SDA	I/O	I2C Data pin.
10	DREAM_SCLK	I	DSP bit clock for I2S
11	AUDIO_IN_2	I	I2S input
12	DREAM_MCLK	I	DSP master clock for I2S.
13	AUDIO_OUT_2	O	I2S output
14	GND	POWER	
15	AUDIO_OUT_3	O	I2S output
16	GND	POWER	

X1 – Archwave uNet Mini Header

Pin	Signal	Direction	Description
1	ARCH_DAC_MUTE	I	0 = normal operation 1 = mute analogue outputs
2	SDATAIN	I	I2S input
3	REQU	O	ARC only: REQU signal
4	SDATA_OUT	O	I2S output

5	ARCH_NRESET_CODEC	I	0 = audio codec reset 1 = normal operation
6	3V3	POWER	
7	I2C0_SCL	O	I2C clock
8	LRCK	O	Wordclock(sample rate)
9	I2C0_SDA	I/O	I2C data
10	SCLK	O	I2S Shift clock
11	96/48	O	0=32, 44.1, 48 kHz 1=64, 88.2, 96 kHz
12	MCLK	O	Audio Master Clock(256fs)
13	GPIO2_4	-	For future use
14	GND	POWER	
15	GPIO4_15	-	For future use
16	GND	POWER	

X2 – Archwave SPI Header

Pin	Signal	Direction	Description
1	SPI_NCS0	O	SPI chip-select, low active
2	SPI_SCK	O	SPI serial clock
3	SPI_MOSI	I/O	SPI data input(slave), SPI data output(master)
4	SPI_MISO	I/O	SPI data input(master), SPI data output(slave)
5	REQU	O	ARC only: REQU signal

X5 – RA Module MCU SPI Header and GPIO pin

Pin	Signal	Direction	Description
1	MCU_SPI_NCS0	I/O	MCU SPI chip-select pin
2	MCU_SPI_SCK	I/O	MCU SPI serial clock pin
3	MCU_SPI_MOSI	I/O	MCU SPI Master-out pin
4	MCU_SPI_MISO	I/O	MCU SPI Master-in pin
5	GPIO	I/O	General Purpose Input/Output pin

X2 – Archwave UART Header

Pin	Signal	Direction	Description
1	3V3	POWER	
2	RXD0	I	UART input to Archwave module
3	TXD0	O	UART output from Archwave module
4	GND	POWER	

P29 – SMTPE811 Expander LED Header

Pin	Signal	Direction	Description
1	3V3	POWER	
2	LD8	O	Expander LED8
3	LD7	O	Expander LED7
4	LD6	O	Expander LED6
5	LD5	O	Expander LED5
6	LD4	O	Expander LED4
7	LD3	O	Expander LED3
8	LD2	O	Expander LED2
9	LD1	O	Expander LED1
10	GND	POWER	

P30 – SMTPE811 Expander Button Header

Pin	Signal	Direction	Description
1	3V3	POWER	
2	ARCH_NRESET_CODEC	I	CODEC reset from Archwave
3	ARC_DAC_MUTE	I	DAC reset from Archwave
4	B3	I	Expander Button 3

5	B4	I	Expander Button 4
6	B5	I	Expander Button 5
7	B6	I	Expander Button 6
8	B7	I	Expander Button 7
9	B8	I	Expander Button 8
10	GND	POWER	

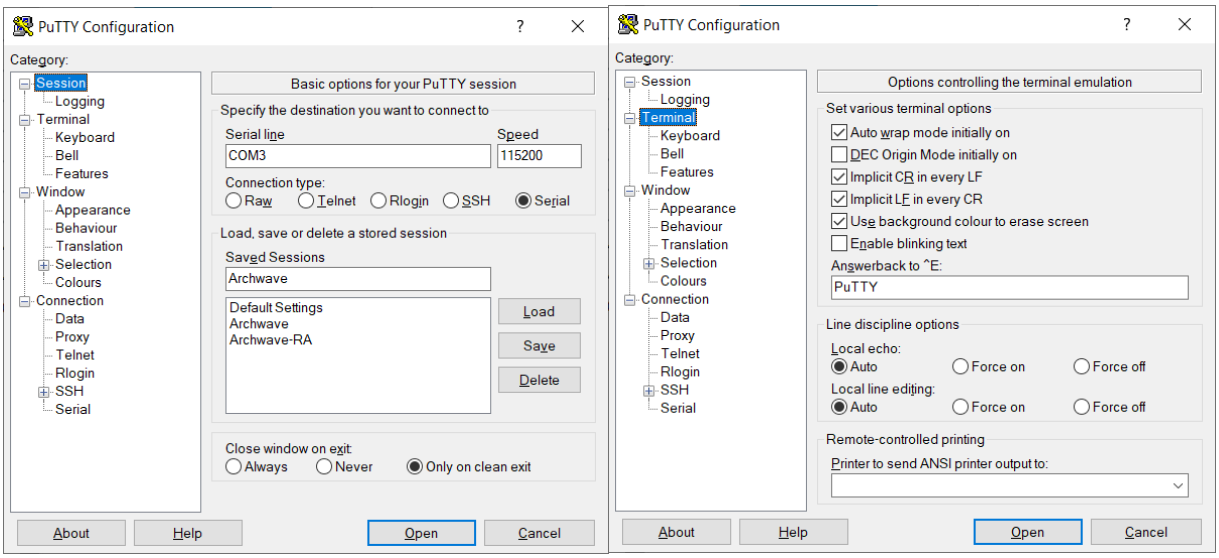
USB

X20 - Archwave USB COM port

For access to the Archwave uNET mini serial connection, use a micro USB cable to connect to a PC and ensure a COM port is established.

Baud rate = 115200, 8 data bits, 1 stop bit, No parity, no flow control

If using Putty, use the following settings.

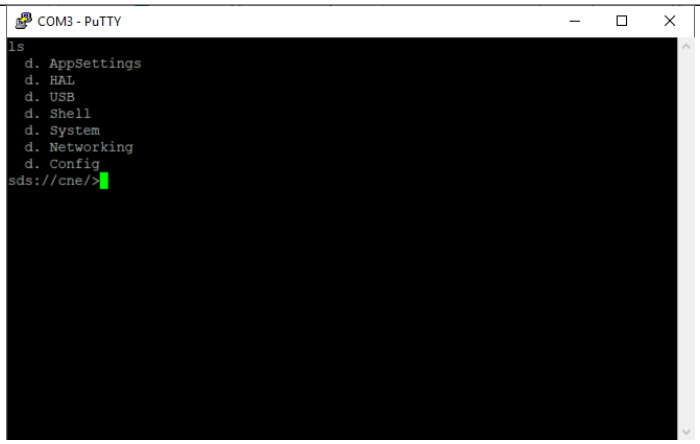


You can then navigate much like in Linux using ‘ls’ and ‘cd’ to display the directories.

d = directory

l = value

To view the currently enabled values. Use 'ls -v'.



To modify a value, for example, changing the streaming interface from ETHERNET to USB, navigate to the correct directory and use:

```
set streamingInterface USB
```

Then reset the uNet module using:

```
sys reset
```

(See Archwave documentation for more details)

X18 –USB (On-The-Go) connection for MCU

Allows access to the MCU's Full Speed USB interface

X19 – Dream connection for USB

Allows control over DSP function using DSP Designer over USB instead of MIDI.

ETHERNET

X22 – RA-ES70DSP04 module Connection to network

X17 – Archwave uNet Mini module connection to network.

POWER

The RA-ES70DSP04-EVM board is configured to fully power all board peripherals, however the situation may arise during development to power down certain parts of the board.

Input is supplied using the included power supply through connector X12. If a replacement is used, provide 12-20V with centre-terminal positive.

Voltage	Header	Jumper	Description
12-20V(VDD)	X12	None	Provides input voltage to board(VDD) and digital 3V3 and 5V supplies
3V3A	X13	1-2 = Disabled 2-3 = Enabled	Enables the 3V3A supply
5VA	X14	1-2 = Disabled 2-3 = Enabled	Enables the 5VA supply
VDD	P34	Present = Enabled Not present = Disabled	Provides power supplies for +15V/-15V for ADC analogue output circuitry
12V	X23	1-2 = Disabled 2-3 = Enabled	Provides +12V power supply for ADC analogue output circuitry
-12V	X24	1-2 = Disabled 2-3 = Enabled	Provides -12V power supply for ADC analogue output circuitry

DAC(U10/U15)

The RA-ES70DSP04-EVM also includes extensive access to the Wolfson WM8740 hardware settings. These have been made available to the user with jumper settings. For greater control. Please refer to the Wolfson WM8740 datasheet for more details.

Header	Function	Jumper	Default Setting
P12/P26	CSBIWO	1-2 = On 2-3 = Off	ON – For 24-bit I2S Data
P11/P25	MODE	1-2 = On 2-3 = Off	OFF – Hardware mode
P8/P22	ML/I2S	1-2 = On 2-3 = Off	ON – I2S
P9/P23	DM1	1-2 = On 2-3 = Off	OFF – Normal Filter Operation

P10/P24	DM0	1-2 = On 2-3 = Off	OFF – De-emphasis mode
P13/P27	MOD8X	1-2 = On 2-3 = Off	OFF – 8X mode disabled
P14/P28	DIFFHW	1-2 = On 2-3 = Off	OFF – Differential mode disabled

AUDIO CONNECTIVITY

Connector	Description
X10	Audio Input 1 - Stereo Audio Input 3.5mm
X11	Audio Input 1 - Stereo Audio Input 3.5mm
X15	Audio Output 1 - Stereo Audio Output 3.5mm
X17	Audio Output 2 - Stereo Audio Output 3.5mm

Balanced Audio Headers

P4 – DAC1(U10) Left Channel

Pin	Signal	Direction	Description
1	AGND	POWER	
2	S+	O	Positive Signal
3	S-	O	Negative Signal
4	AGND	POWER	

P7 – DAC1(U10) Right Channel

Pin	Signal	Direction	Description
1	AGND	POWER	
2	S+	O	Positive Signal
3	S-	O	Negative Signal

4	AGND	POWER	

P18 – DAC2(U15) Left Channel

Pin	Signal	Direction	Description
1	AGND	POWER	
2	S+	O	Positive Signal
3	S-	O	Negative Signal
4	AGND	POWER	

P21 – DAC2(U15) Right Channel

Pin	Signal	Direction	Description
1	AGND	POWER	
2	S+	O	Positive Signal
3	S-	O	Negative Signal
4	AGND	POWER	

Physical Dimensions(mm)