TCD6000

6 CHANNEL CLASS-T DIGITAL AUDIO PROCESSOR USING DIGITAL POWER PROCESSING™ TECHNOLOGY

Technical Information – Preliminary **Revision 0.97 – June 2003**

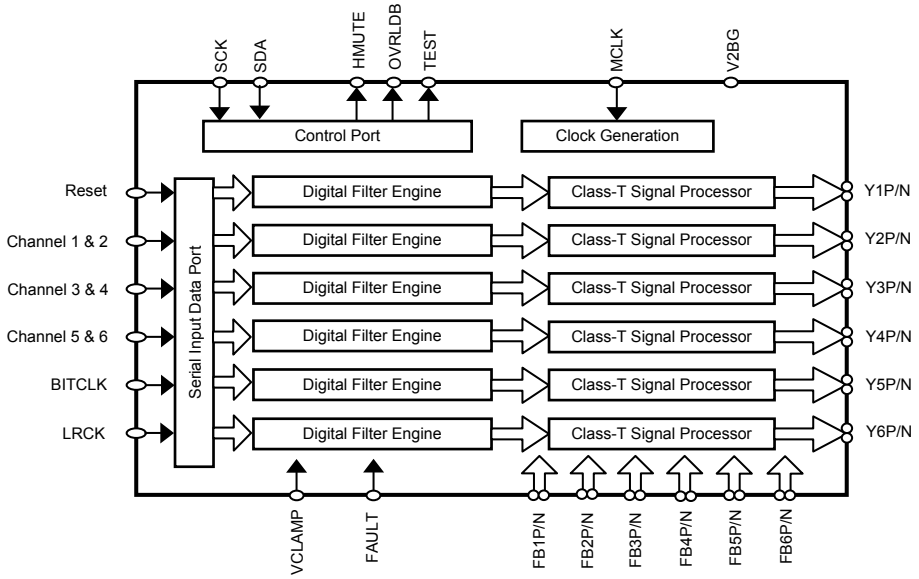
General Description

The TCD6000 is a high-performance 6-channel digital audio amplifier processor. It receives 6 digital audio channels (3 pairs) and outputs 6 complementary single-bit digital data streams suitable for driving Tripath or other switching output stages.

The TCD6000 accepts data at audio sample rates ranging from 32kHz to 192kHz and incorporates digital interpolation and sigma-delta conversion to produce streamed digital output signals. When combined with switching output stages, the TCD6000 allows the implementation of a complete digital audio system incorporating Class-T Digital Audio Amplification.

Features

- Class-T architecture combining ultra-low distortion with high efficiency
- Inputs support I^2S and other PCM audio formats
- Up to 24-bit resolution (16, 18, 20, and 24 bit)
- 100dB dynamic range
- THD+N less than 0.03%
- Input sampling rates up to 192kHz
- Standard 2-wire control interface
- Stereo headphone amplifier
- Digital volume control
  - 120dB range
  - 1/2 dB step size in 1/8 dB increments
  - Zero crossing detection for click free transitions
  - Optional mute mode leaves headphone amplifiers operating
- Automatic DC offset cancellation
- Digital de-emphasis filtering for 32, 44.1 and 48kHz sampling rates



Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	Max	UNITS
VD50	5V Digital Power Supply	-0.3	6.0	V
VD33	3.3V Digital Power Supply	-0.3	4.0	V
VA50	5V Analog Power Supply	-0.3	6.0	V
VA33	3.3V Analog Power Supply	-0.3	4.0	V
Vlogic3	Input Logic Level (DATAx, MCK, BITCLK, LRCLK, SCK, SDA, RESET, ADDRx)	-0.3	VD33+0.3	V
Vlogic5	Input Logic Level (VCLAMP, FBxx, FAULT)	-0.3	VD50+0.3	
TA	Operating Free-air Temperature Range	-40	85	°C
T_{STORE}	Storage Temperature Range	-55	150	°C
T_{JMAX}	Maximum Junction Temperature		150	°C
ESD_{HB}	ESD Susceptibility – Human Body Model (Note 2) All pins		2000	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. See the table below for Operating Conditions.
Note 2: Human body model, 100pF discharged through a 1.5KΩ resistor.

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VD50	5V Power Supply	4.5	5	5.5	V
VD33	3.3V Power Supply	3.0	3.3	3.6	V
V_{HI-3}	Vlogic3 Input High	2		VD33	V
V_{LO-3}	Vlogic3 Input Low	0		0.8	V
V_{HI-5}	Vlogic5 Input High	VD50-1.0		VD50	V
V_{LO-5}	Vlogic5 Input Low	0		1.0	V
T_A	Operating Temperature Range	-40	25	85	C

Note 3: Recommended Operating Conditions indicate conditions for which the device is functional. See Digital, Analog, and Switching Characteristics for guaranteed specific performance limits.

Power and Thermal Characteristics

T_A = 25 °C. Unless otherwise noted, the MCK frequency is 12.288 MHz and the measurement bandwidth is 20kHz. See Application/Test Circuit on page 8.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PTOTAL	Total Power Dissipation	VD30 = 3.3V VD50 = 5.0V		350		mW
ID50	VD50 Power Supply Current	VD50 = 5.0V		50		mA
ID33	VD33 Power Supply Current	VD33 = 3.3V		30		mA
θ_{JC}	Junction-to-case Thermal Resistance			1.0◦	C/W	
θ_{JA}	Junction-to-ambient Thermal Resistance (still air)			20◦	C/W	

Digital Characteristics

T_A = 25 °C. Unless otherwise noted, the MCK frequency is 12.288 MHz and the measurement bandwidth is 20kHz. See Application/Test Circuit on page 8.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIH33	High-Level Input Voltage	VD33 = 3.3V	TBD		TBD	V
VIL33	Low-Level Input Voltage	VD33 = 3.3V	TBD		TBD	V
VIH5	High-Level Input Voltage	VD50 = 5.0V	TBD		TBD	V
VIL5	Low-Level Input Voltage	VD50 = 5.0V	TBD		TBD	V
VOH33	High-Level Output Voltage	VD33 = 3.3V	TBD			V
VOL33	Low-Level Output Voltage	VD33 = 3.3V			TBD	V
VOH5	High-Level Output Voltage	VD50 = 5.0V	4.0			V
VOL5	Low-Level Output Voltage	VD50 = 5.0V			0.5	V

Analog Characteristics

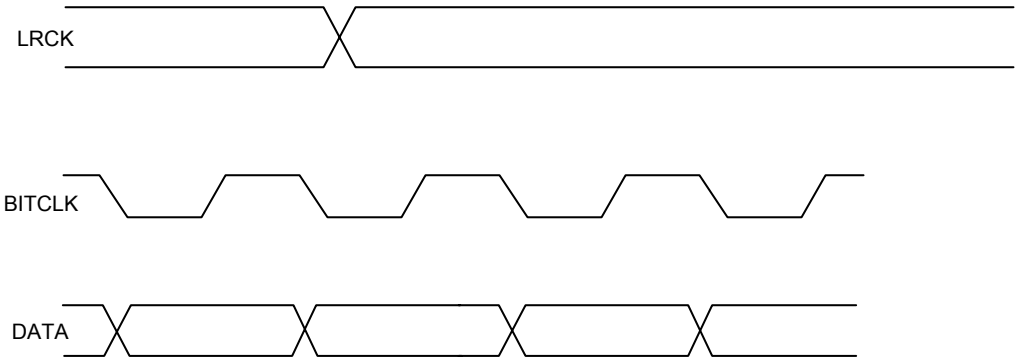
T_A = 25 °C. Unless otherwise noted, the MCK frequency is 12.288 MHz and the measurement bandwidth is 20kHz. See Application/Test Circuit on page 8.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution					24	Bits
THD + N	Total Harmonic Distortion Plus Noise	Fs = 44.1kHz		TBD		dB
DR	Dynamic Range	Fs = 44.1kHz		TBD		dB
SNR	Signal-to-Noise Ratio	Fs = 44.1kHz		TBD		dB
CS	Inter-Channel Separation			TBD		dB
PSR	Power Supply Rejection			TBD		dB
A_V	Amplifier Gain		-128	0	18	dB
A_{VERROR}	Channel to Channel Gain Error	P_{OUT} = 10W/Channel, R_L = 4Ω See Application / Test Circuit			0.5	dB
PB	Passband	Fs = 44.1kHz	0		20	kHz
SB	Stopband	Fs = 44.1kHz	24.1			kHz

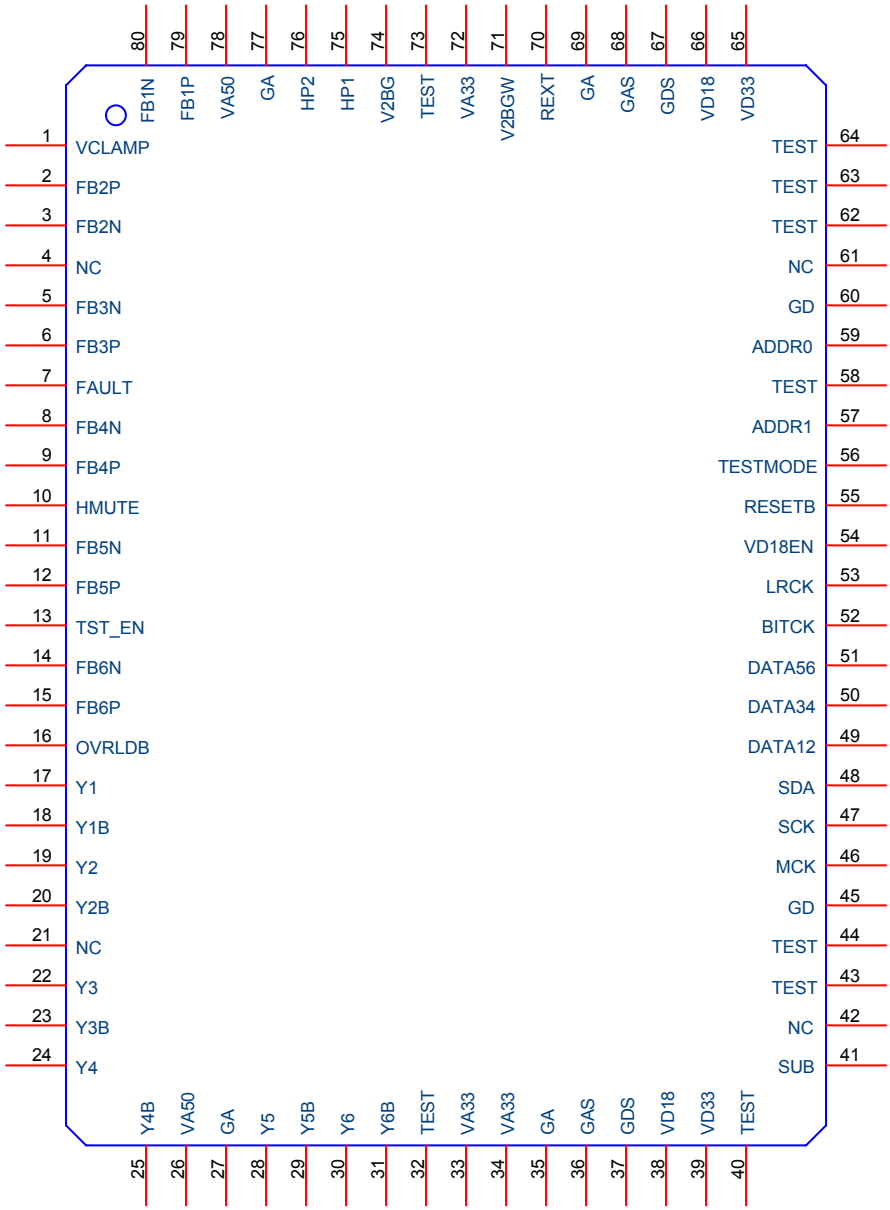
Switching Characteristics

T_A = 25 °C. Unless otherwise noted, the MCK frequency is 12.288 MHz and the measurement bandwidth is 20kHz. See Application/Test Circuit on page 8.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Master Clock Timing					
fMCK	Frequency		8.192		24.56	MHz
	Duty Cycle		40		60	%
	Left-Right Clock Timing					
fLRCK	1X Mode		32	44.1	48	KHz
	2X Mode			96		KHz
	4X Mode			192		kHz
	Serial Interface Timing					
tBITCK	BITCK period					
	1X Mode		488.2	354.3	325.5	ns
	2X Mode			177.1		ns
	4X Mode			88.6		ns
	Control Interface Timing					
tSCK	SCK Period		200			ns
tSCKL	SCK Pulse Width Low		80			ns
tSCKH	SCK Pulse Width High		80			ns
tSDAset	SDA Setup Time		40			ns
tSDAhold	SDA Hold Time		40			ns
tSDA rise	SDA Rise Time				20	ns
tSDAfall	SDA Fall Time				20	ns



TCD6000 Pin Layout

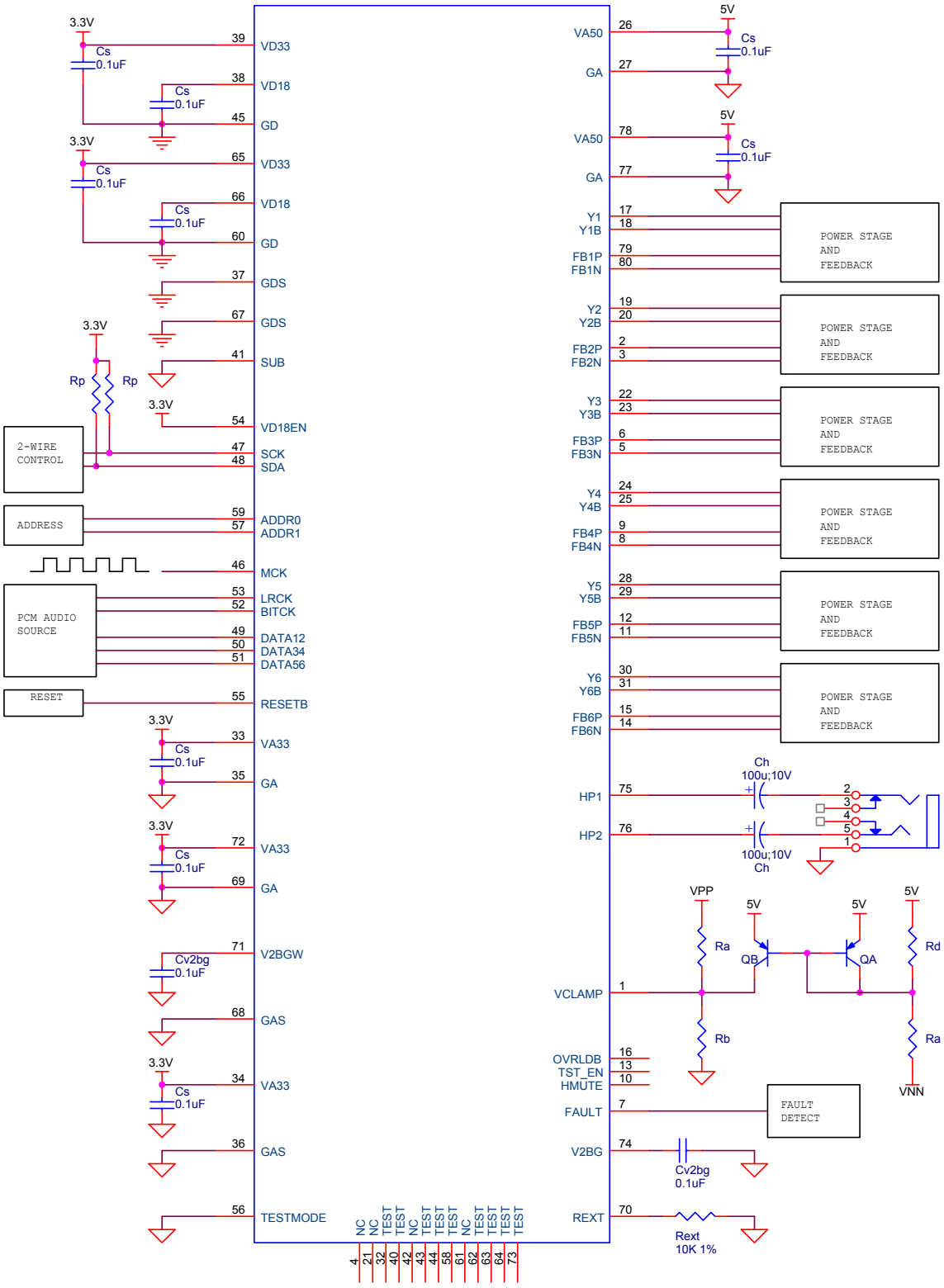


TCD6000 Pin Description

Pin	Function	Description
1	VCLAMP	Soft clamp threshold voltage input to control audio signal clipping
2	FB2P	Switching feedback
3	FB2N	Switching feedback
4	NC	No connect
5	FB3N	Switching feedback
6	FB3P	Switching feedback
7	FAULT	3-level digital input to detect power stage fault condition
8	FB4N	Switching feedback
9	FB4P	Switching feedback
10	HMUTE	Digital output – indicates processor channels are muted
11	FB5N	Switching feedback
12	FB5P	Switching feedback
13	TST_EN	Digital output to put power stage in to test mode
14	FB6N	Switching feedback
15	FB6P	Switching feedback
16	OVRLDB	Digital output – indicates that one or more channels are near saturation
17	Y1	Switching modulator output
18	Y1B	Switching modulator output
19	Y2	Switching modulator output
20	Y2B	Switching modulator output
21	NC	No connect
22	Y3	Switching modulator output
23	Y3B	Switching modulator output
24	Y4	Switching modulator output
25	Y4B	Switching modulator output
26	VA50	5V analog power supply
27	GA	Analog ground
28	Y5	Switching modulator output
29	Y5B	Switching modulator output
30	Y6	Switching modulator output
31	Y6B	Switching modulator output
32	TEST	Test pin – must be kept floating
33	VA33	3.3V analog power supply
34	VA33	3.3V analog power supply
35	GA	Analog ground
36	GAS	Analog substrate
37	GDS	Digital substrate
38	VD18	1.8V digital power supply
39	VD33	3.3V digital power supply
40	TEST	Test pin – must be kept floating
41	SUB	Package substrate
42	NC	No connect
43	TEST	Test pin – must be kept floating
44	TEST	Test pin – must be kept floating
45	GD	Digital ground
46	MCK	Master clock digital input
47	SCK	2-wire interface clock input
48	SDA	2-wire interface serial data input
49	DATA12	PCM audio input for channels 1 and 2
50	DATA34	PCM audio input for channels 3 and 4
51	DATA56	PCM audio input for channels 5 and 6
52	BITCK	PCM audio bit clock input
53	LRCK	PCM audio left/right clock input
54	VD18EN	1.8V internal regulator enable
55	RESETB	Reset input – resets all internal registers
56	TESTMODE	Test mode enable – must be kept grounded
57	ADDR1	Chip address select 1
58	TEST	Test pin – must be kept floating
59	ADDR0	Chip address select 0
60	GD	Digital ground
61	NC	No connect
62	TEST	Test pin – must be kept floating
63	TEST	Test pin – must be kept floating
64	TEST	Test pin – must be kept floating
65	VD33	3.3V digital power supply

66	VD18	1.8V digital power supply
67	GDS	Digital substrate
68	GAS	Analog substrate
69	GA	Analog ground
70	REXT	Analog current reference input – requires 10K ohms +/- 1% to GA supply
71	V2BGW	Reference Voltage
72	VA33	3.3V analog power supply
73	TEST	Test pin – must be kept floating
74	V2BG	Reference Voltage
75	HP1	Headphone amplifier output channel 1
76	HP2	Headphone amplifier output channel 2
77	GA	Analog ground
78	VA50	5V analog power supply
79	FB1P	Switching feedback
80	FB1N	Switching feedback

TCD6000 Connection Diagram



TCD6000 Operation Overview

POWER SUPPLY

The TCD6000 requires both 3.3V and 5V supplies. Pins labeled VD33 correspond to the digital power networks, and pins labeled VA33 and VA50 correspond to the analog power networks. Pins labeled VAIO33 power the internal 3.3V analog busses and should be connected to the analog 3.3V supply. All should be separately decoupled to their respective grounds.

All TCD6000 logic inputs are 3.3V unless otherwise specified.

SUB

SUB is the package substrate. It should be tied to GA.

VD18EN

VD18EN is a logic input that enables the internal 1.8V regulator. It should be tied to VD33.

REXT

The REXT pin should be connected to ground through an external 10KΩ. This connection is used by the TCD6000 as a current reference. The 10KΩ resistor must have an accuracy of +/- 1%.

V2BG and V2BGW

The V2BG and V2BGW pin should each be AC coupled to GA with a 0.1uF capacitor.

RESETB

When pulled low, the RESET pin will force all control registers to their default state.

FAULT

The TCD6000 has no fault detection circuitry of its own. Over/under voltage, over current, and over temperature fault detection are expected to be done externally. A FAULT input has been provided as an alternate "mute" input, however. The default (non-muted) state for FAULT is floating wherein the pin will self-bias to approximately 2.5V. If FAULT is taken to either 5V or 0V the TCD6000 will latch into the muted state. The TCD6000 will remain latched in this FAULT-based muted condition until the FAULT pin is released (floated) and a hard mute (see register 2Ch) has been asserted and then cleared.

I2S INPUTS AND CLOCKS

The TCD6000 receives PCM digital audio data in I2S format or variations thereof. The format consists of an audio data input (DATAn), a bit clock (BITCK) and a 1x clock (LRCK). In addition, a master clock (MCK) synchronizes all digital operations inside the device. Each DATAn input carries serial data for 2 channels. The LRCK clock differentiates between odd and even channel data. When LRCK is in one logic state, it reads odd channel data; when LRCK is in the opposite logic state, it reads even channel data. BITCK is synchronized with the serial data input, and latches data on either rising edges or falling edges of BITCK (programmable option).

The TCD6000 has 3 serial data inputs (DATA1, DATA2, and DATA3) and therefore can receive 6 channels of audio data. The group of bits received on a DATAn input during a half period of LRCK clock is called a PCM data sample. It is a 2’s complement representation of the amplitude of sound on that channel at that time.

There are 32 pulses of BITCK for every half period of LRCK. So, in theory, it is possible to read up to 32 bits of data per sample. However, only a maximum of 24 bits are read. The device will also accept 16, 18, and 20 bit formats depending on what has been specified in the control registers.

The TCD6000 can operate in 3 different modes: 1X, 2X and 4X. These modes correspond to the frequency at which data samples are received.

In the 1X mode, data samples can be received at 32 kHz, 44.1 kHz, or 48 kHz.
In the 2X mode, data samples can be received at 96 kHz.
In the 4X mode, data samples can be received at 192 kHz.

A specific operating mode must be programmed into the proper control register (address 22h).
The MCK clock frequency must be set according to the operating mode as follows:

- In 1X mode, MCK clock must have 256 pulses per data sample.
- In 2X mode, MCK clock must have 128 pulses per data sample.
- In 4X mode, MCK clock must have 64 pulses per data sample.

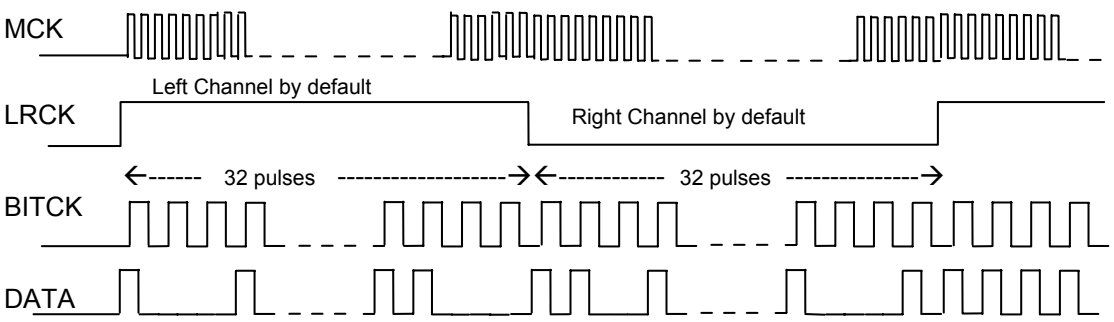
The phase of MCK is not critical, as long as the frequency is correctly set. The duty cycle of MCK should be between 48% and 52%.

When the HFR bit (register 23h, bit D3) is set to '1', the TCD6000 divides MCK by 2 so that higher frequency system clocks may be used. In this case, the division automatically creates a 50% duty cycle internal clock.

The following table shows the MCK clock frequency for each operating mode:

Data sampling rate	32 kHz	44.1 kHz	48 kHz	96 kHz	192 kHz
MCK frequency (HFR = '0')	8.192 MHz	11.289 MHz	12.288 MHz	12.288 MHz	12.288 MHz
MCK frequency (HFR = '1')	16.384 MHz	22.578 MHz	24.576 MHz	24.576 MHz	24.576 MHz

The following diagram shows the waveforms of the different clocks in the TCD6000:



2-WIRE INTERFACE

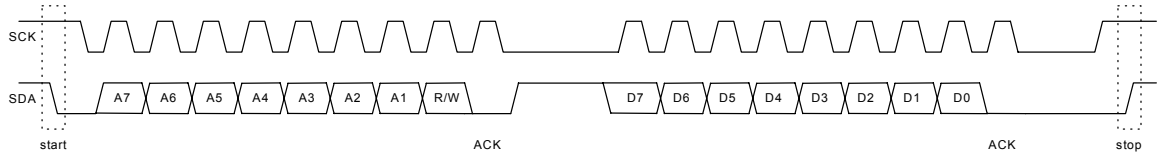
The 2-wire interface is a simple bi-directional bus interface for allowing a microcontroller to read and write control registers in the TCD6000. Every component hooked up to the 2-wire bus has its own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and/or transmitter depending on its functionality. The TCD6000 acts as a slave while a microcontroller would act as a master.

The TCD6000 device address is 80h, 82h, 84h, or 86h depending on the state of the ADDRn pins. The TCD6000 constantly monitors the 2-wire data input and waits until its device address appears before writing into or reading from its control registers. The 8th bit of the address determines whether the master is reading or writing. When the last bit is HIGH, the master is reading from a register on the slave. When the last bit is LOW, the master is writing to a register on the slave.

ADDR1	ADDR0	TCD6000 write address	TCD6000 read address
0	0	80h	81h
0	1	82h	83h
1	0	84h	85h
1	1	86h	87h

The 2-wire interface consists of a serial data input (SDA) and a clock input (SCK) and is capable of both reading and writing. Both SCK and SDA are bidirectional lines connected to VD33 via a pull-up resistor. When the bus is free both lines are HIGH.

The SCK clock frequency is typically less than 400 kHz. Data is transmitted serially in groups of 8 bits, followed by an acknowledge bit. The data on the SDA line is expected to be stable while SCK is HIGH.



A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master. Data transfer with acknowledge is obligatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received. The receiver can hold the SCK line LOW after an acknowledge to force the transmitter to wait until the receiver is ready to accept another byte.

When addressed as a slave, the following protocol must be adhered to, once a slave acknowledge has been returned, an 8-bit sub-address will be transmitted. If the LSB of the slave address was ‘1’, a repeated START condition will have to be issued after the address byte; if the LSB is ‘0’ the master will transmit to the slave with direction unchanged.

When the master writes data to the slave, the following events occur:

0. SDA and SCK are both HIGH.
1. A start condition is generated when the master pulls SDA LOW.
2. The master begins toggling SCK and transmits the slave’s device address on SDA with a 0 in the LSB (ex. 80h).
3. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.
4. The slave holds SCK low until it is ready to receive the next byte.
5. The slave releases SCK and the master begins toggling SCK and transmits the control register address on SDA.
6. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.

7. The slave holds SCK low until it is ready to receive the next byte.
8. The slave releases SCK and the master begins toggling SCK and transmits the data byte on SDA.
9. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.
10. The slave holds SCK low until it is ready to receive the next byte.
11. To transmit data to subsequent control registers, repeat steps 8 through 10.
12. A stop condition is generated when SCK is released and SDA goes HIGH while SCK is still high.

When the master reads data from the slave, the following events occur:

0. SDA and SCK are both HIGH.
1. A start condition is generated when the master pulls SDA LOW.
2. The master begins toggling SCK and transmits the slave's device address on SDA with a 1 in the LSB (ex. 81h).
3. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.
4. The slave holds SCK low until it is ready to receive the next byte.
5. The slave releases SCK and the master begins toggling SCK and transmits the control register address on SDA.
6. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.
7. The slave holds SCK low until it is ready to transmit data.
8. The slave releases SCK and the master begins toggling SCK and the slave transmits the data byte on SDA.
9. On the ninth SCK pulse, the slave releases SDA and the master acknowledges by pulling SDA LOW.
10. The slave holds SCK low until it is ready to transmit the next byte.
11. To transmit data from subsequent control registers, repeat steps 8 through 10.
12. A stop condition is generated when SCK is released and SDA goes HIGH while SCK is still high.

Control Registers

This section describes the user-programmable registers controlling many features of the TCD6000. They are programmed using the 2-wire interface.

Control bits shown in gray are for Tripath use only and should be set to the values shown. All registers not shown should not be changed.

Activating the external Reset input sets all control registers to their default values. Other internal reset modes always preserve the contents of these registers.

Control Register Mapping

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	Mute Status	0	0	0	MUS	SMU	FMU	HMU	AMU
01h	Volume Status	0	0	VZ6	VZ5	VZ4	VZ3	VZ2	VZ1
20h	Freeze Control	0	0	0	0	0	0	0	CHG
21h	Filter Bypass Control	DCB	DEB	DRB	0	0	0	0	0
22h	Sampling Rate Control	0	0	0	1Xf	1Xs	0	4X	2X
23h	Operation Control	0	1	CA1	CA0	HFR	R2	R1	R0
24h	Digital Input Format	0	DP	BCK	CCK	I2S	DA	DW1	DW0
25h	Channel 1 Volume	V17	V16	V15	V14	V13	V12	V11	V10
26h	Channel 2 Volume	V27	V26	V25	V24	V23	V22	V21	V20
27h	Channel 3 Volume	V37	V36	V35	V34	V33	V32	V31	V30
28h	Channel 4 Volume	V47	V46	V45	V44	V43	V42	V41	V40
29h	Channel 5 Volume	V57	V56	V55	V54	V53	V52	V51	V50
2Ah	Channel 6 Volume	V67	V66	V65	V64	V63	V62	V61	V60
2Bh	Volume Ramp Rate	RR7	RR6	RR5	RR4	RR3	RR2	RR1	RR0
2Ch	Channel Mute Control	M3R	M3L	M2R	M2L	M1R	M1L	HM	AM
2Dh	Auto-Mute Timing	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
2Eh	Volume Change Control	0	0	0	0	VR1	VR0	VRE	ZCE
39h	Dither Control	0	DT6	DT5	DT4	DT3	DT2	DT1	DT0
73h	Output Delay Control	0	0	0	0	YD3	YD2	YD1	YD0
74h	Test Control	0	HMP	HPO	TO	0	0	0	0
76h	Output Timing Control	DEL	DCB	0	0	STB	BB2	BB1	BB0
77h	Hard Mute Control	0	H3R	H3L	H2R	H2L	H1R	H1L	0
78h	Gain Control	GN1	0	0	0	0	0	0	0
7Ah	Gain Control	GN2	0	0	0	0	0	0	0
7Bh	Gain Control	GN6	GN5	GN4	GN3	0	0	0	0
7Dh	Force Offset and B Cal Control	FO1	BC6	BC5	BC4	BC3	BC2	BC1	FO0

Mute Status Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	Mute Status	0	0	0	MUS	SMU	FMU	HMU	AMU
Default		0	0	0	0	0	0	0	0

This is a read only register that indicates the status of various mute conditions. A '1' indicates that that particular mute is active.

AMU = Auto Mute
HMU = Hard Mute
FMU = Fault Mute
SMU = Smart Mute

MUS is the logical OR of D3..D1. If any of the above mute states are active, MUS will be set to '1'.

Volume Status Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01h	Volume Status	0	0	VZ6	VZ5	VZ4	VZ3	VZ2	VZ1
Default		0	0	0	0	0	0	0	0

These are read only bits that are set to '1' when their respective volume registers are cleared to 0. For example, when register 27h has a value of 8Ch, VZ3 is cleared to '0'. When register 27h has a value of 00h, VZ3 is set to '1'.

Freeze Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20h	Volume Status	0	0	0	0	0	0	0	CHG
Default		0	0	0	0	0	0	0	0

While CHG is set to '1', any value that is written to a register takes effect immediately. However, while CHG is cleared to '0', any changes that are made to registers will not take effect until CHG is set to '1'. For example, if the user wanted to set all channels to a volume of F6h at the same time, the user could clear CHG, set registers 25h through 2Ah to F6h one at a time, then set CHG to '1'.

Filter Bypass Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
21h	Filter Bypass Control	DCB	DEB	DRB	0	0	0	0	0
Default		0	0	0	0	0	0	0	0

This register allows users to bypass any of the 3 digital filters incorporated in the TCD6000:

DCB = DC blocking filter
DEB = De-Emphasis filter
DRB = Droop correction filter

A setting these bits to '1' bypasses the corresponding filter.

The DC blocking filter eliminates the DC component in an incoming signal. The frequency response of the DC blocking filter is shown in Figure 1 for the 1X, 2X, and 4X modes.

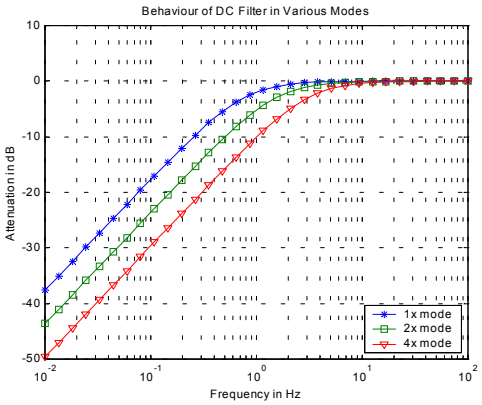


Figure 1. DC Blocking Filter Characteristics

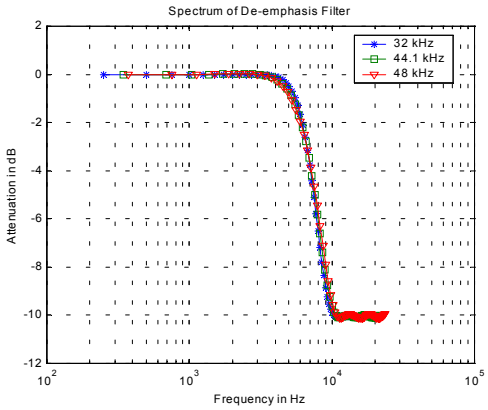


Figure 2. De-Emphasis Filter Characteristics

The De-Emphasis filter is used to re-shape the frequency response and reduce gain for frequencies above 3.183 kHz. It is only available in the 1X mode. If enabled, it needs to be selected for 1 of 4 possible input data rates (32 kHz, 44.1kHz, or 48 kHz), as specified by bits D4 and D3 in the Sampling Rate and De-Emphasis Control Register (address 22h).

The frequency response of the De-emphasis filter is shown in Figure 2 for all 3 input data rates.
The De-Emphasis Filter Selection bit is ignored for the 2X and 4X input data-sampling modes.

A Droop correction filter is included in the TCD6000 to correct for droop and ripple in the frequency response of the entire signal processing chain. The frequency response of the droop filter for the 1X, 2X, and 4X sampling modes is shown below.

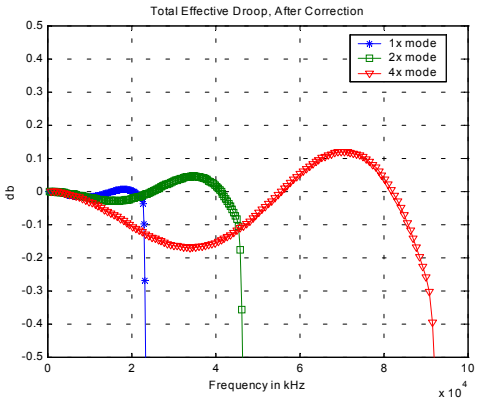


Figure 3. Frequency response of the Droop Correction Filter

Sampling Rate Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22h	Sampling Rate Control	0	0	0	1Xf	1Xs	0	4X	2X
Default		0	0	0	0	0	0	0	0

This register allows the user to specify the data-sampling mode (1X, 2X or 4X). When the 1X mode is selected and the de-emphasis filter is enabled, 1Xf and 1Xs select between 32 kHz, 44.1kHz, and 48 kHz de-emphasis filters.

Bits 4X	2X	
0	0	1X mode (32 kHz, 44.1 kHz, or 48 kHz)
0	1	2X mode (96 kHz)
1	0 or 1	4X mode (192 kHz)

Bits 1Xf	1Xs	
0	0	data-sampling rate is 44.1 kHz
0	1	data-sampling rate is 32 kHz
1	0	data-sampling rate is 48 kHz
1	1	not used

If the 2X or the 4X modes are selected, the de-emphasis filter is automatically disabled, and the setting of bit D6 in the Filter Bypass Control register (address 21h) will be ignored.

Operation Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
23h	Operation Control	0	1	CA1	CA0	HFR	R2	R1	R0
Default		0	1	0	0	0	1	1	1

This register allows the user to specify 2 operational characteristics of the TCD6000:

- The internal reset mode (control bits R0 thru R2)
- The High Frequency Master Clock option (control bit HFR)

If the Left/Right channel clock (LRCK) and Bit clock (BITCK) are not properly synchronized with the Master clock (MCK), R0, R1, and R2 control the internal reset mode as follows:

[D2..D0]	Action
xx0	None
001	Reset only
011	Reset with hard Mute
101	Reset with soft Mute
111	Reset with hard and Soft Mute

R0 enables an internal reset if clocks are not properly synchronized. This internal reset will clear all internal registers and incoming input data, except the control registers, which retain their contents. Since incoming data is cleared, sound immediately turns off upon an internal reset.
This reset is different from an external reset, which is created by pulling the RESETB pin low. An external reset will reset ALL registers of the TCD6000, including the control registers.

R1 enables a “Hard-mute” upon internal reset. A Hard-mute will set all 12 differential outputs to ground (Y and YB outputs) and minimize power consumption in the power stages. When the internal reset condition is removed, an auto-calibration will take place before the outputs are restored.

R2 enables a “Soft-mute” upon internal reset. A Soft-mute will leave all outputs switching but all sound will be muted.

It is recommended to leave all 3 bits (R0, R1, and R2) at their default value of "1" under normal operating conditions.

The Master Clock (MCK) frequency can be either nominal (8.192MHz to 12.288MHz) or double (16.384MHZ to 24.576 MHz). Internally, the master clock must run at the nominal rate. A divide-by-two must be enabled when the MCK frequency is too high. This is accomplished by setting HFR to '1'. See the section on"I2S Inputs and Clocks" for more info.

CA1 and CA0 control internal DC offset alignment and should be set to '0' and '1' respectively.

Digital Input Format Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24h	Digital Input Format	0	DP	BCK	CCK	I2S	DA	DW1	DW0
Default		0	0	1	0	1	0	1	1

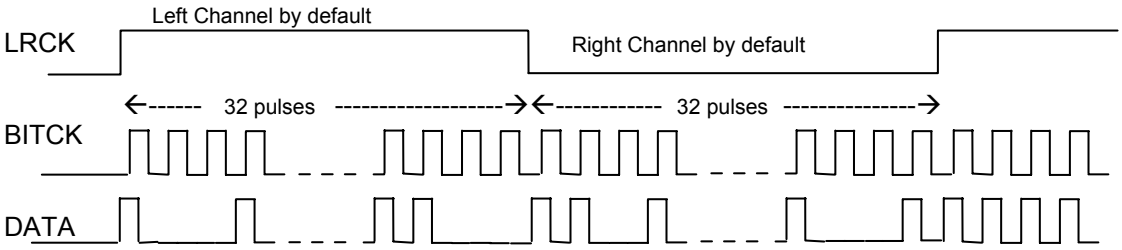
This register allows the user to specify the following digital interface characteristics:

- Input data width (DW0 and DW1))
- Input data alignment with respect to LRCK clock edges (DA)
- Polarity of the LRCK clock (CCK)
- Polarity of the BITCK clock (BCK)
- Polarity of the input data (DP)

DW1 and DW0 define the input data width. Any data outside of the selected data width will be ignored.

DW1	DW0	Input Data Width
0	0	16 bit
0	1	18 bit
1	0	20 bit
1	1	24 bit

The serial input data is aligned to the edges of the Left/Right channel clock (LRCK). A Bit Clock (BITCK) provides individual bit synchronization. Data can be read on the rising or falling edge of BITCK. The BITCK frequency is 64 times higher than the LRCK frequency, so that BITCK has 32 pulses for each half of a LRCK period. This provides a capability to read up to 32 data bits. Depending on the Input Data Width defined, only 16 to 24 of these bits are read.



The most significant bit of data always arrives first and the least significant bit last. Data can be left aligned or right aligned to the LRCK clock. If data is left aligned, the most significant bit of data arrives at the beginning of the LRCK half-period. If data is right aligned, the least significant bit of data arrives just before the end of the LRCK half-period.

DA specifies the Data Alignment scheme. When DA is '0', data is left aligned to LRCK transitions. When DA is '1', data is right aligned to LRCK transitions.

If data is left aligned, the most significant bit of data can arrive on the first or the second BITCK pulse. The I2S format specifies that it arrive on the second BITCK pulse. When the I2S control bit is '1', the data is conforming to the I2S standard, i.e. the most significant data bit is read during the second BITCK pulse. When the I2S control bit is '0', the most significant data bit is read during the first BITCK pulse.

If data is right aligned, the I2S control bit has no effect.

When CCK is '0', even channel data is read while LRCK is high and odd channel data is read while LRCK is low. When CCK is '1', odd channel data is read while LRCK is high and even channel data is read while LRCK is low.

When BCK is '1', data is latched on the falling edge of BITCK. When BCK is '0', data is latched on the rising edge of BITCK.

DP is used to specify the polarity of the 2's complement audio data. If DP is '0', the data is non-inverted. If DP is '1', the data is inverted.

Channel Volume Registers

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
25h	Channel 1 Volume	V17	V16	V15	V14	V13	V12	V11	V10
26h	Channel 2 Volume	V27	V26	V25	V24	V23	V22	V21	V20
27h	Channel 3 Volume	V37	V36	V35	V34	V33	V32	V31	V30
28h	Channel 4 Volume	V47	V46	V45	V44	V43	V42	V41	V40
29h	Channel 5 Volume	V57	V56	V55	V54	V53	V52	V51	V50
2Ah	Channel 6 Volume	V67	V66	V65	V64	V63	V62	V61	V60
Default		0	0	0	0	0	0	0	0

The TCD6000 has 6 channel volume registers, one for each channel. The 8-bit value in each register represents the volume loudness for the corresponding channel. The least significant bit, D0, represents a volume increment of 0.5dB. Therefore the total range available is 128dB. Maximum volume is achieved when the volume register contains a value of FFh, and no sound is heard if its value is 00h.

In addition, a coarse adjustment of the volume (1X, 2X, 4X, and 8X) is made possible by programming the Volume Change Control Register.

Volume Ramp Rate Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2Bh	Volume Ramp Rate	RR7	RR6	RR5	RR4	RR3	RR2	RR1	RR0
Default		1	0	0	0	0	0	0	0

The TCD6000 can be programmed to have volume changes take effect immediately or be ramped at a predefined rate for all channels. If the Volume Ramp Enable bit is set, the Volume Ramp Rate Register defines the ramp rate.

Although the Volume Control Registers define the channel volume within an accuracy of ½ dB, volume will be ramped internally in 1/8 dB steps when ramping is enabled.

The number entered into the Volume Ramp Rate Register can be from 0 (00h) to 255 (FFh). If the number entered is N, the time delay between two consecutive 1/8 dB volume increments is equal to:

N x (4 periods of LRCK)

As an example, if N = 100 and data samples are coming in at a 44.1kHz rate, the period of LRCK is 22.67usec. The delay between two consecutive 1/8 dB volume increments is:

100 x 4 x 22.67usec = 9068usec

Therefore if the volume change is 60 dB (480 increments of 1/8 dB), the total ramp time will be:

480 x 9068usec = 4.32 second

Channel Mute Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2Ch	Channel Mute Control	M6	M5	M4	M3	M2	M1	HM	AM
Default		0	0	0	0	0	0	1	0

The TCD6000 has 3 different Mute functions: Soft-Mute, Hard-Mute, and Auto-Mute.

The **Soft-Mute** function will turn off volume selectively on any of the 6 channels. Setting control bits M1 through M6 to '1' will issue a Soft-Mute on the corresponding channels. If the Volume Ramp Enable bit in the Volume Change Control Register is set, the volume will ramp down at a rate defined by the Volume Ramp Rate Register. When in soft mute, all differential outputs (Y1P and Y1N through Y6P and Y6N) are still switching. Resetting bits M1L through M3R to '0' will re-establish volume on the corresponding channels. The rate at which the volume will ramp up depends on the Volume Ramp Enable settings.

The **Hard-Mute** function is enabled by setting control bit HM high. This function starts with a Soft-Mute on all channels simultaneously. Once volume is turned off on all channels, all differential outputs (Y1 and Y1B through Y6 and Y6B) stop switching. This will reduce power consumption in the power stages driven by the TCD6000.

When control bit HM is reset to '0', the Hard-Mute condition is removed, and the TCD6000 goes through an automatic calibration cycle. Once the calibration cycle is complete, volume is re-established on all channels at a rate defined by the Volume Ramp Enable settings.

The **Auto-Mute** function is enabled by setting the AM bit to '1'. This function detects digital silence (all data input bits at 0) on all 6 channels lasting more than a pre-defined delay. It then issues a Hard-Mute. The delay is determined by the contents of the Auto-Mute Timing Register (described below). Upon arrival of non-zero data on any channel, the Hard-Mute condition is automatically removed. The volume on all 6 channels is re-established at a rate defined by the Volume Ramp Enable settings. The Auto-Mute function reduces power consumption in the power stages during periods of silence.

Auto-Mute Timing Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2Dh	Auto-Mute Timing	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Default		0	0	0	0	0	0	0	0

This register is only used if the Auto-Mute function is enabled. Its contents specify the duration of silence on all 6 channels before a Hard-Mute condition is issued. If the number entered is "N", the duration of silence is equal to:

$$(2N + 1) \times (1{,}048{,}576 \text{ periods of LRCK})$$

As an example, if N = 1 and the period of LRCK is 22.67usec, the period of silence required before a Hard-Mute condition is issued is:

$$3 \times 1{,}048{,}576 \times 22.67\text{usec} = 71.3 \text{ seconds}$$

Volume Change Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2Eh	Volume Change Control	0	0	0	0	VR1	VR0	VRE	ZCE
Default		0	0	0	0	0	1	0	0

This register is used to specify 3 characteristics of volume change for all channels:

- Coarse volume range (control bits VR0 and VR1)
- Volume ramp enable (control bit VRE)
- Zero-crossing enable (control bit ZCE)

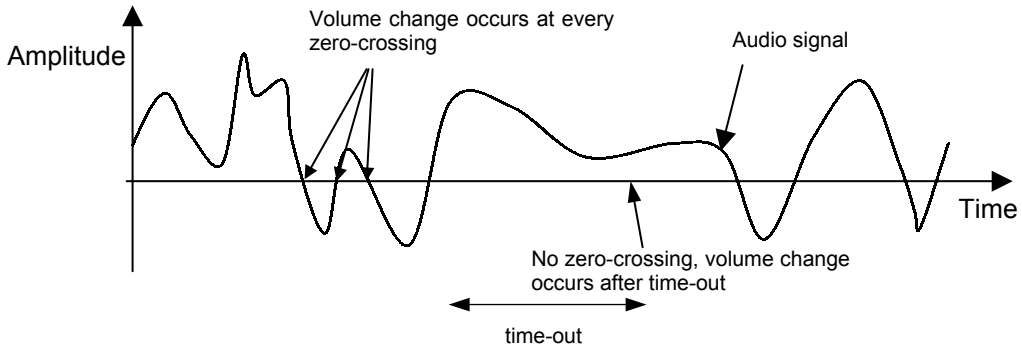
A coarse adjustment of the volume is made possible by selecting one of four combinations for bits VR0 and VR1.

Bits VR1	VR0	
0	0	1X volume
0	1	2X volume
1	0	4X volume
1	1	8X volume

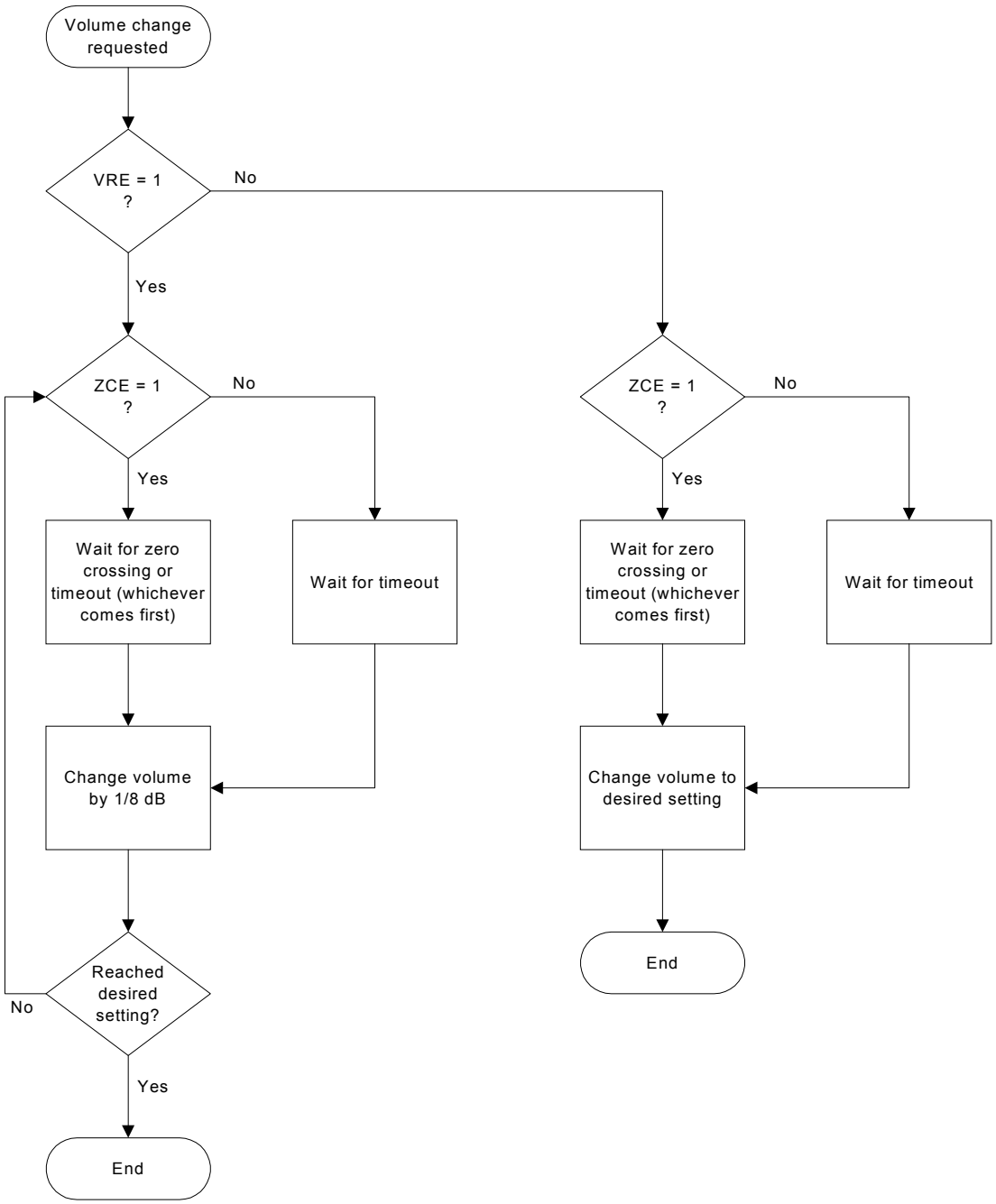
This coarse volume adjustment affects all 6 channels globally.

The VRE control bit is the Volume Ramp Enable bit. If VRE = '1', the contents of the Volume Ramp Rate Register will be read and determine how fast the volume can ramp up or down on all 6 channels. Refer to the Volume Ramp Rate Register section for a more detailed explanation of how the ramp rate is calculated.

The ZCE control bit is the Zero-Crossing Enable bit. A polarity inversion on the audio input signal is called a "Zero-Crossing". Changing volume only at Zero-Crossings helps to avoid popping sounds. If ZCE is set to '1', volume will only be allowed to change at Zero-Crossings. However, if a Zero-Crossing does not occur within a time defined by the Volume Ramp Rate Register (called "time-out" in the graph below), volume will change anyway. If the Zero-Crossing feature is enabled, the VRE control bit will still control whether the volume change occurs in one large step or in 1/8 dB steps at Zero-Crossings.



Volume Change Flowchart



Dither Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
39h	Dither Control	0	DT6	DT5	DT4	DT3	DT2	DT1	DT0
Default		0	0	0	0	0	0	0	0

This register is used to set the amount of dither in the system. It should be set to 3Ch for normal operation.

Output Delay Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
73h	Output Delay Control	0	0	0	0	YD3	YD2	YD1	YD0
Default		0	0	0	0	0	0	0	0

The loop delay of each Class-T amplification channel can be selectively increased by programming this 4-bit field. It used to control the maximum output switching frequency. Each channel receives the same amount of additional delay which defaults to 15nS but can be increased from 15nS to 240nS in 15nS steps.

YD<3:0>	Actual count	Processor Y-output delay
0000 (POR default)	1	15 nS
0001	2	30 nS
0010	3	45 nS
0011	4	60 nS
0100	5	75 nS
0101	6	90 nS
0110	7	105 nS
0111	8	120 nS
1000	9	135 nS
1001	10	150 nS
1010	11	165 nS
1011	12	180 nS
1100	13	195 nS
1101	14	210 nS
1110	15	225 nS
1111	16	240 nS

Truth table for Y-output delay control.

Test Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
74h	Test Control	0	HMP	HPO	TO	0	0	0	0
Default		0	0	0	0	0	0	0	0

Setting the TO control bit to '1' forces the TST_EN output pin to go high. This pin can be used to put the power stage IC into test mode. If the power stage does not have a TST_EN input, the TST_EN output can be used as a general purpose logic output.

The HPO control bit HPO immediately stops all switching without muting the headphone amplifier outputs.

The HMP bit controls whether the HMUTE output is active high or active low. Setting HMP to '1' causes the HMUTE output to be active low.

Output Timing Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
76h	Output Timing Control	DEL	DCB	0	0	STB	BB2	BB1	BB0
Default		0	0	0	0	0	0	0	0

Control bits BB0 through BB2 are used to program a “Break before Make” delay in the Y outputs.

“Break before Make” is a dead time at the Y-outputs where both Y and YB of each channel are low together for a period of time in order to prevent shoot-through current in the output power MOSFET devices.

BB<2:0>	BBM Delay
000	0 nS
001	15 nS
010	30 nS
011	45 nS
100	60 nS
101	75 nS
110	90 nS
111	105 nS

Break before make (BBM) delay table

The STB control bit enables a 16-bit Startup Burst for driving bootstrapped output stages.

The DCB control bit should be set to ‘1’ if a bridged output stage is being used. DCB should be cleared to ‘0’ if a single ended output stage is being used.

The DEL control bit enables the on-chip delay compensation. Delay compensation should be enabled when using bootstrapped output stages.

Gain Control Registers

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
78h	Gain Control	GN1	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0
7Ah	Gain Control	GN2	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0
7Bh	Gain Control	GN6	GN5	GN4	GN3	0	0	0	0
Default		0	0	0	0	0	0	0	0

When the GNn control bits are cleared to ‘0’, the TCD6000 operates in low gain mode. In this mode, the noise floor is lowered but the system may not be able to obtain the maximum power output from the power stage. When the GNn control bits are set to ‘1’, the TCD6000 operates in high gain mode. In this mode, gain is increased by 25%. The system will now be able to obtain the maximum power output from the power stage but the noise floor will have increased accordingly.

The automatic DC offset cancellation settings will have been affected by changes in gain. If gain is changed, hard mute should be cycled to prevent DC offset at the outputs and possible power supply pumping.

Force Offset B Cal Control Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
7Dh	Force Offset and B Cal Control	FO1	BC6	BC5	BC4	BC3	BC2	BC1	FO0
Default		0	0	0	0	0	0	0	0

The BCn control bits should be set to '1' if a bridged output stage is being used. The BCn bits should be cleared to '0' if a single ended output stage is being used.

The FO1 and FO0 bits should be set to '1' for proper DC offset compensation.

OUTPUT CHARACTERISTICS

The TCD6000 outputs consist of six pairs of complementary 1-bit digital data streams, one pair per audio channel. They switch from 0V to 5V (+/- 10%) and constitute a pulse-density-modulated (PDM) form of the audio signal. They are used to drive Tripath power stages in a switching amplifier configuration.

The output power of a power stage can be expressed as V^2/R, V being the voltage amplitude of the power stage output and R the speaker input impedance, typically 4 to 8 ohms.

The audio signal is recovered by filtering the PDM signal through an LC filter located at the inputs of the speaker. The following figure shows the power stage output waveform and the filtered signal at the speaker inputs:

Typical waveform at power stage output

Typical waveform at speaker inputs after LC filtering

TCD6000 outputs are pulse density modulated outputs. Their frequency varies constantly over time and can typically reach a maximum value of 800 kHz.

A Mute output (HMUTE) can be connected to all 6 power stages to force them into a tri-state mode when a hard mute condition is encountered. The HMUTE output can be programmed to be either active-high or active-low (bit D6 in control register 74h).

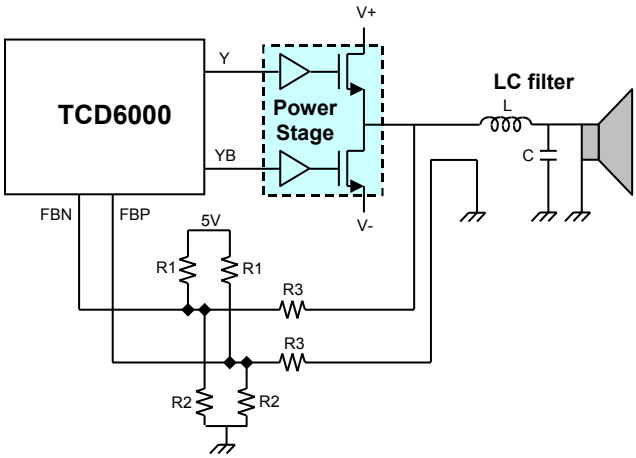
An overload is detected whenever the combination of input signal amplitude and volume programmed in the TCD6000 results in output signal saturation and distortion. The OVRLDB pin goes active low when this condition occurs.

A test output pin is also provided (TST_EN) for external testing purposes. Setting bit D4 in control register 74h will force this output to an active high state.

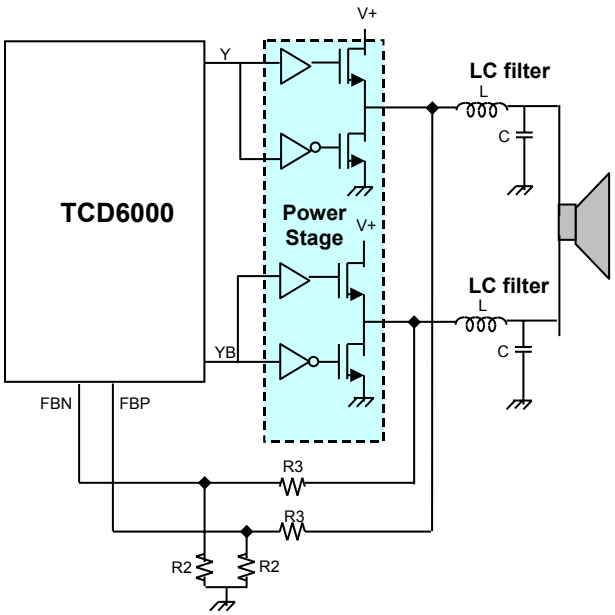
The HMUTE, OVRLDB and TST_EN outputs are 5V digital outputs.

The TCD6000 also includes a pair of stereo headphone outputs (HP1 and HP2), which are connected to channels 1 and 2. These outputs are analog with maximum 3V peak-to-peak amplitude. They have a common mode voltage of 2V and should therefore be AC coupled to the headphone jack.

FEEDBACK CONNECTIONS



Feedback network for single ended configurations (1 channel shown)



Feedback network for bridged configurations (1 channel shown)

Differential feedback from the power stage outputs to the TCD6000 FB inputs is required. This feedback is taken directly from the outputs of the power stage, before the LC filter stage. It allows the TCD6000 to compensate for power stage distortion (non-linearity, power supply noise, etc.) and to deliver an ultra-low THD that is unique to class-T technology. Total harmonic distortion is typically less than 0.03% with most power stages.

Resistors R1, R2, and R3 create a voltage divider structure to reduce the unfiltered output of the power stage for the feedback pins. In bridged configurations, R1 is absent (infinity).

The peak to peak switching voltage seen at V(FBP) - V(FBN) should be approximately 3.5V when V+ and V- (or V+ alone in a bridged system) are at their nominal values. It should not exceed 4.5V.

Neither V(FBP) nor V(FBN) should be allowed to exceed Vcc.

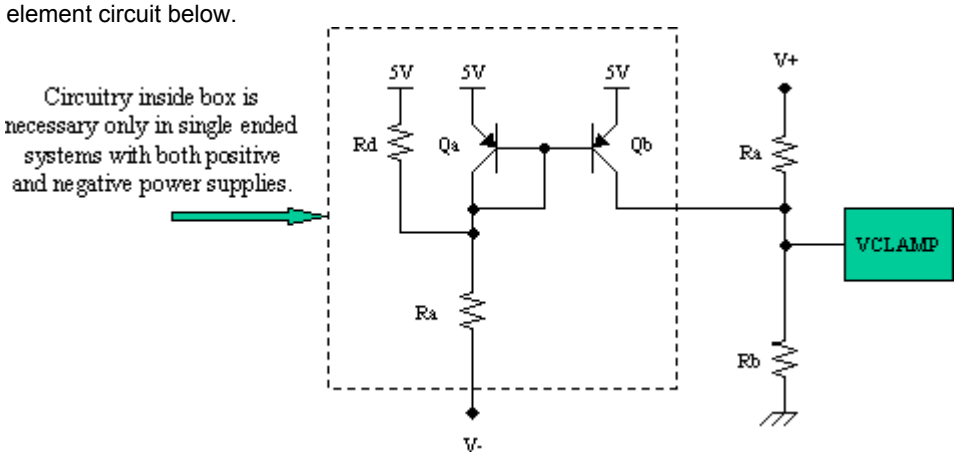
Neither V(FBP) nor V(FBN) should be allowed to go below ground.

The pair of resistors which share the name R1 should match each other to 1% or better. The same applies to the R2 resistor pair and the R3 resistor pair. Mismatching between these like-named resistors will result in a degradation in PSRR.

It is recommended that the parallel combination of R1 and R2 be 500 ohms to 1k ohms. If this value is lower than 500 ohms, R3 will need to be relatively low and will experience unnecessary power dissipation. If the parallel combination of R1 and R2 is significantly higher than 1k ohms, the pole at the feedback nodes formed by this resistance and parasitic capacitances may drop to a frequency low enough to negatively effect loop stability.

VCLAMP PIN BIASING

The VCLAMP pin must have a DC voltage applied which is proportional to the peak to peak voltage swing of the power output switching stage in the amplifier system. More explicitly, the potential at VCLAMP should be 0.525 times the peak to peak differential voltage seen at each channel's *feedback* pins (i.e., the full final value voltage swing neglecting any RC settling time effects). This means that the component values used in the circuitry biasing the VCLAMP pin are a direct function of the chosen feedback network components. In a full bridged system, proper VCLAMP biasing is achieved via a simple two resistor divider between V+ (the output stage power supply) and ground, shown in the right-hand portion of the circuit below (excluding the portion in the dotted line box). In a single ended (half bridge) system, VCLAMP biasing is achieved by the entire six element circuit below.



In a bridged system, stated in terms of the components described in the feedback section, the values for Ra and Rb are determined as follows (Rd = 0.176 x Ra):

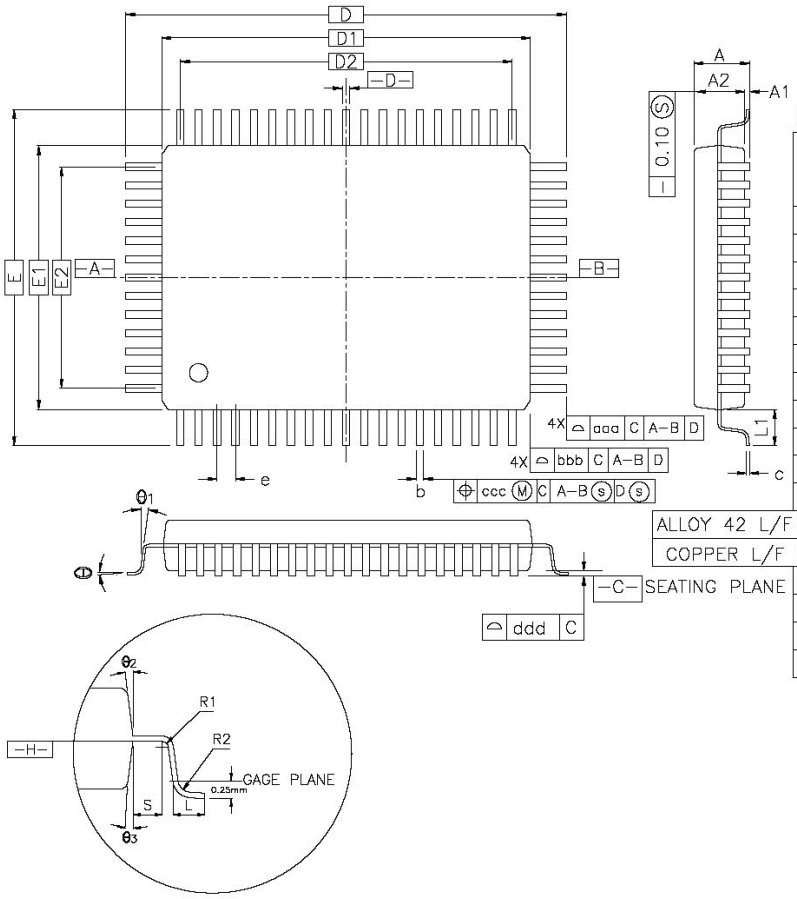
$$Ra = Rb \times \left(\frac{0.952 \times R3}{R2||25k} - 0.048 \right)$$

where R2||25k is the parallel combination of R2 and 25k Ohms. In a single ended (half bridge) system, the component value relationships would be, stated in terms of the components in the feedback section:

$$Ra = Rb \times \left(\frac{1.90 \times R3}{R1||R2||25k} + 0.90 \right)$$

where Rd = 0.176 x Ra, and R1||R2||25k is the parallel combination of R1, R2, and 25k Ohms.

Package Information



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
ALLOY 42 L/F θ2 , θ3	7° REF			7° REF		
COPPER L/F θ2 , θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L 1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	64L						80L						100L						128L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.35	0.40	0.50	0.014	0.016	0.020	0.30	0.35	0.45	0.012	0.014	0.018	0.22	0.30	0.38	0.009	0.012	0.015	0.170	0.200	0.270	0.007	0.008	0.011
e	1.00 BSC.			0.039 BSC.			0.80 BSC.			0.031 BSC.			0.65 BSC.			0.026 BSC.			0.50 BSC.			0.020 BSC.		
D2	18.00 REF			0.709 REF			18.40 REF			0.724			18.85 REF			0.742			18.50			0.728		
E2	12.00 REF			0.472 REF			12.00 REF			0.472			12.35 REF			0.486			12.50			0.492		
TOLERANCES OF FORM AND POSITION																								
aaa	0.25			0.010			0.25			0.010			0.25			0.010			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.20			0.008			0.20			0.008			0.13			0.005			0.08			0.003		
ddd	0.10			0.004			0.10			0.004			0.10			0.004			0.08			0.003		

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

PRELIMINARY – This product is still in development. Tripath Technology Inc. reserves the right make any changes without further notice to improve reliability, function or design.

This data sheet contains the design specifications for a product in development. Specifications may change in any manner without notice. Tripath and Digital Power Processing are trademarks of Tripath Technology Inc. Other trademarks referenced in this document are owned by their respective companies.

Tripath Technology Inc. reserves the right to make changes without further notice to any products herein to improve reliability, function or design. Tripath does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

TRIPATH'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN CONSENT OF THE PRESIDENT OF TRIPATH TECHNOLOGY INC.
As used herein:
1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in this labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Contact Information

TRIPATH TECHNOLOGY, INC
2560 Orchard Parkway, San Jose, CA 95131
408.750.3000 - P
408.750.3001 - F

For more Sales Information, please visit us @ www.tripath.com/cont_s.htm
For more Technical Information, please visit us @ www.tripath.com/data.htm